Semiconductor Memory And Method For Controlling The Same
Inventor's Name: FUJIOKA, et al.
Application No.: New
Docket No.: 107337-00051

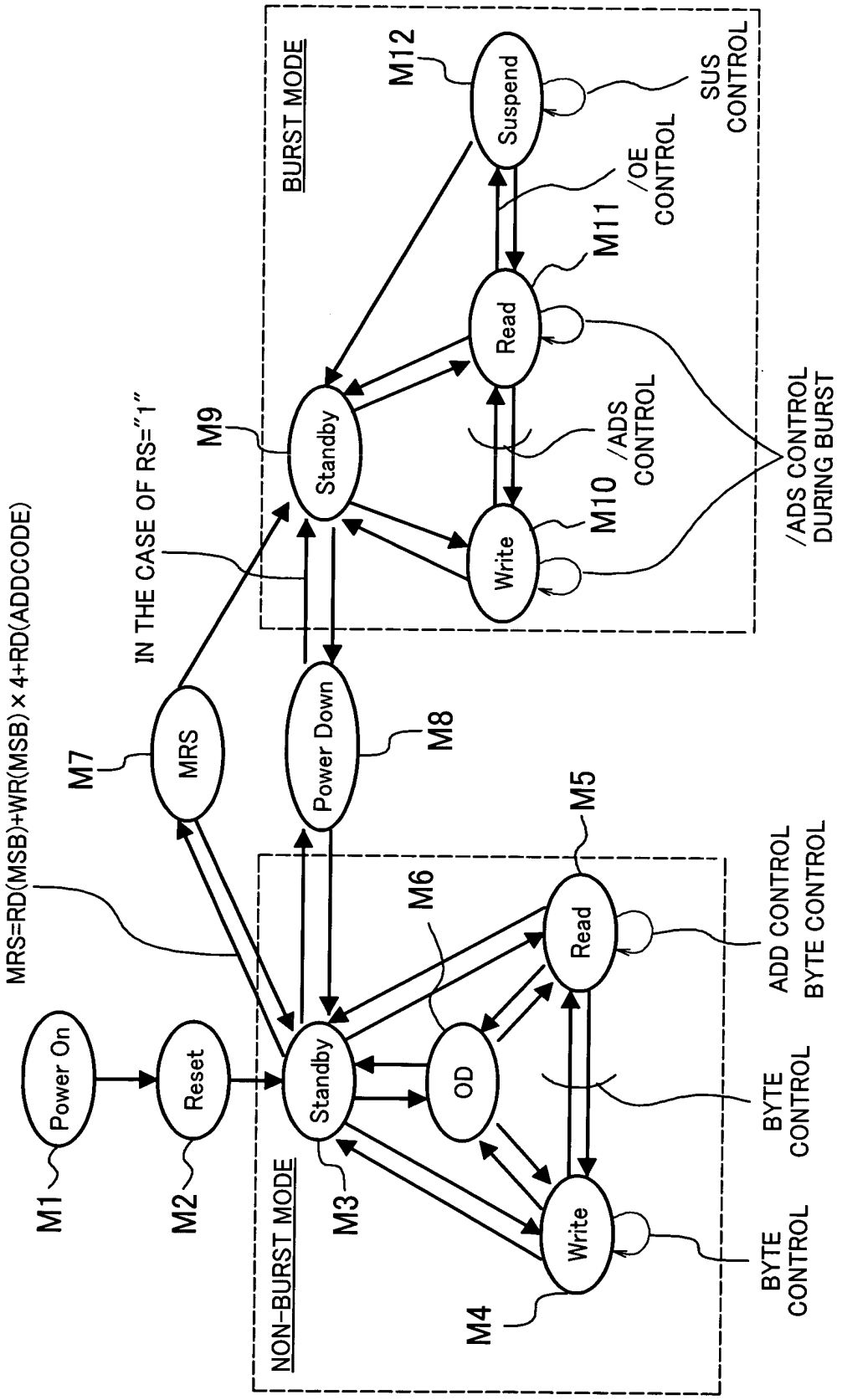

FIG. 1

Controlling The Same
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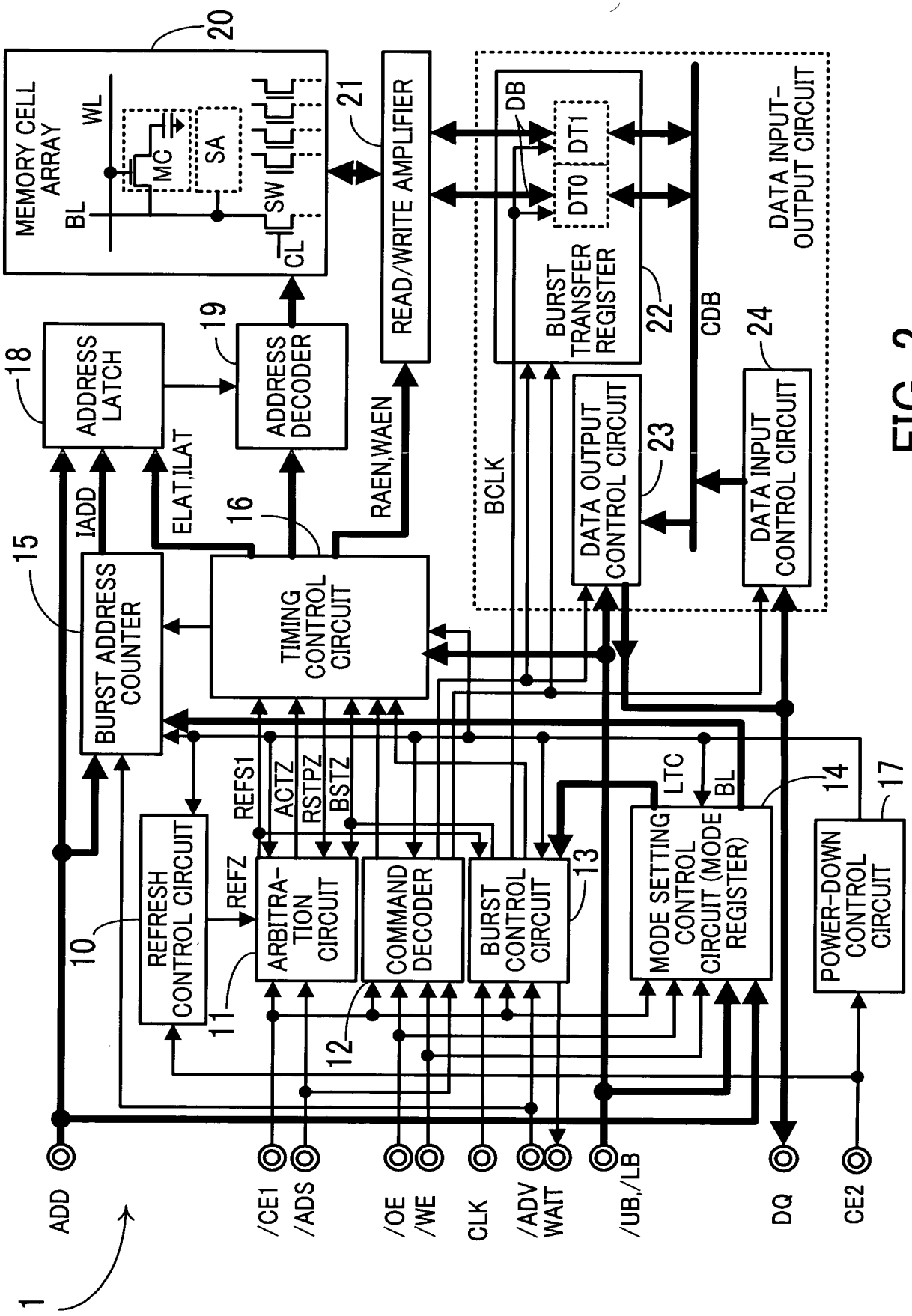

FIG. 2

FIG. 3A

Add.	20	19	18	17	16	15	14	13	12
Func.	Partial Mode		Data Length		Mode	Read Latency Count			Reset
Sym.	PM		DL		MD	RLC			RS

FIG. 3B

Name	Description
PM	00 :16M 01 :8M 10 :Full Chip 11 :0M(Def.)
DL	00 :8word burst 01 :16word burst 10 :32word burst 11 :Continuous burst
MD	0 :Synchronous Burst Enabled 1 :Asynchronous Page Enabled(Def.)
RLC	000 :Latency Count=2 001 :Latency Count=3 010 :Latency Count=4 011 :Latency Count=5
RS	0 :Reset Enabled(Def.) 1 :Reset Disabled

MODE	CE2	/CE1	/OE	/WE	/ADS	/LB	/UB	DQ_{0-7}	DQ_{8-15}	Retention
Power Down/Reset	L	H	X	X	X	X	X	HiZ	HiZ	No/Partial
Standby	H	H	X	X	X	X	X	HiZ	HiZ	Yes
Output Disable	H	L	H	H	X	X	X	HiZ	HiZ	Yes
Read	H	L	L	H	X	L	L	Dout	Dout	Yes
No Read	H	L	L	H	X	H	H	HiZ	HiZ	Yes
Lower Byte Read	H	L	L	H	X	L	H	Dout	HiZ	Yes
Upper Byte Read	H	L	L	H	X	H	L	HiZ	Dout	Yes
Write	H	L	X	L	X	L	L	Din	Din	Yes
Abort Write	H	L	X	L	X	H	H	Invalid	Invalid	Yes
Lower Byte Write	H	L	X	L	X	L	H	Din	Invalid	Yes
Upper Byte Write	H	L	X	L	X	H	L	Invalid	Din	Yes
Illegal	H	L	L	L	X	X	X	---	---	---

FIG. 4

FIG. 5A

sequence	1st	2nd	3rd	4th	5th	6th
CMD	RD	WR	WR	WR	WR	RD
Add	MSB	MSB	MSB	MSB	MSB	CODE

FIG. 5B